Agilent Technologies

"Turning RF IC technology into successful design"

Satellite Tuner Single Chip Simulation with Advanced Design System

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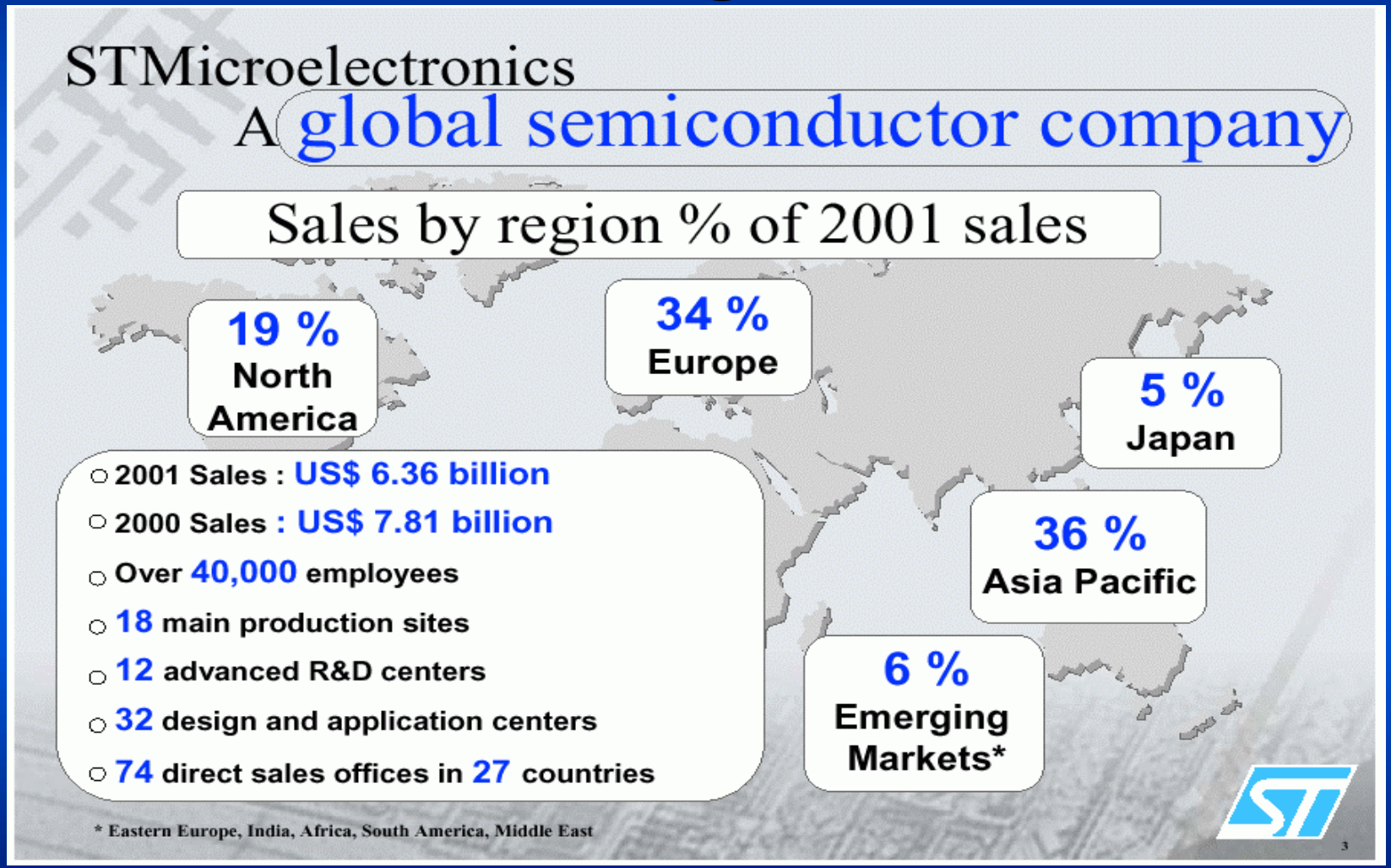
STMicroelectronics

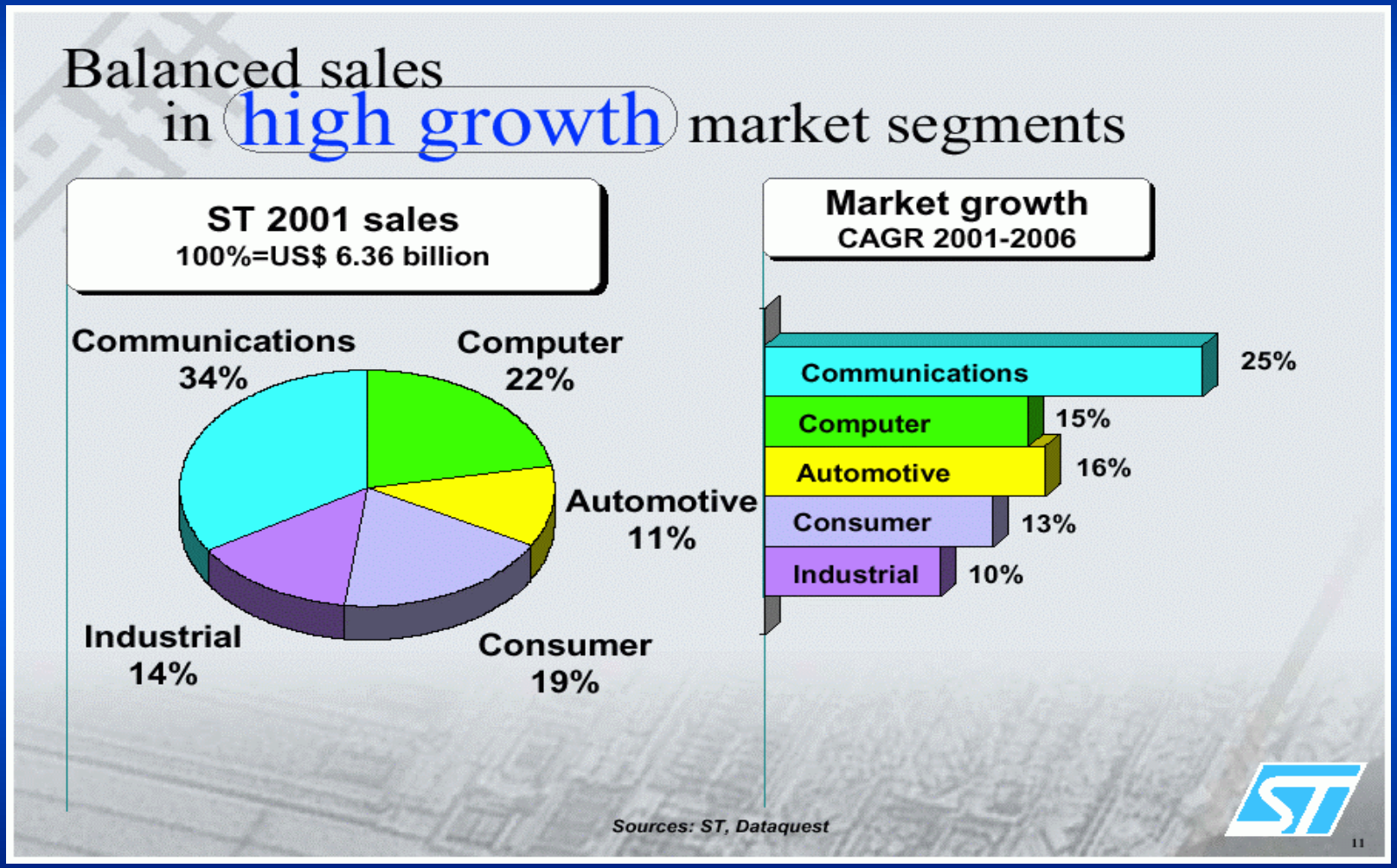
Outline

- STMicroelectronics at a glance
- STV0399 satellite tuner description
- ADS platform
- Simulation results
- What we learnt

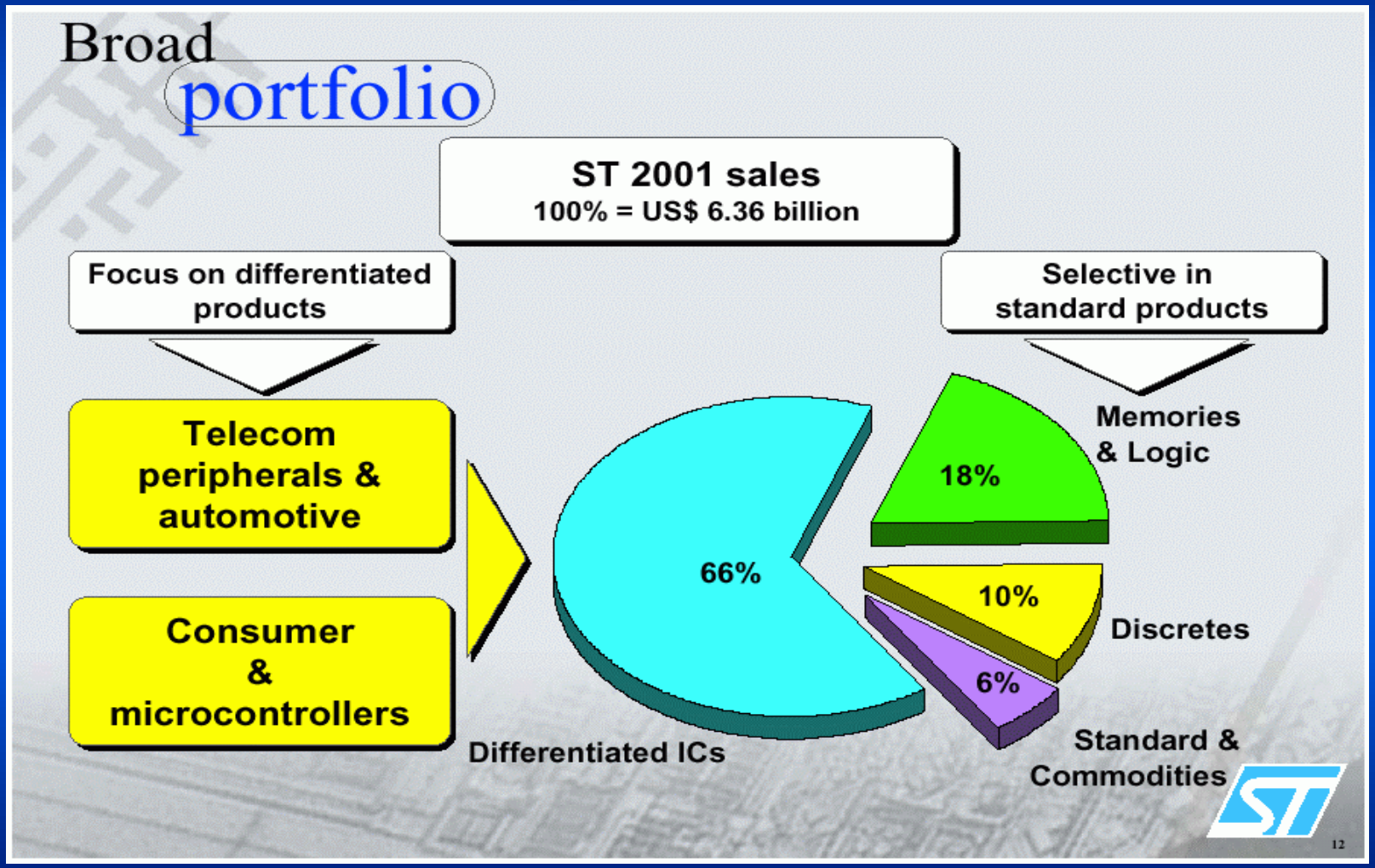
ST in figures



ST market segments



ST portfolio



ST applications

Complete product solutions for high growth applications

Priority segments


Computer peripherals


Digital consumer


Automotive


Communications


Smart cards

Focus applications

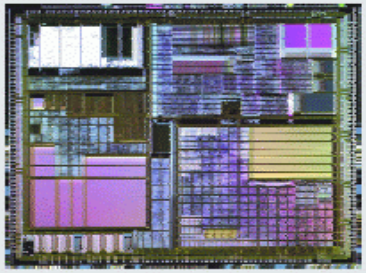
- Data storage
- Printers and imaging
- Monitors and displays
- Webcam
- Optical Mouse
- Set-top boxes
- DVDs
- Digital TVs
- Digital cameras
- MP3 players
- Engine/body/safety
- Car radio
- Car multimedia
- Telematics
- Wireless
- Networking
- Telephone
- Banking
- User ID
- Security

14

ST and SOCs

A pioneer and leader in system-on-chip solutions

- System know-how
- Strategic alliances
- Broad IP portfolio
- Powerful engines DSP & MCU cores



- Broad range of technologies
- World-class volume manufacturing
- Software expertise
- Design methodology

Delivering SOCs to market

13

ADS ST design kit deliveries

0.35u	0.25u	0.18u		0.13u	
BiCMOS6G	BiCMOS7	RFCMOS8	HCMOS8D	HCMOS9GP	BiCMOS9
6.0	3.0	4.0	1.0	5.0	1.0
Available				Under development	
IFF + Dynamic Link + ADS schematic capture				Dynamic Link version only	

Outline

- STMicroelectronics at a glance
- **STV0399 Satellite Tuner description**
  - Specifications, Architecture, Layout, Board
- ADS platform
- Simulation results
- Conclusion

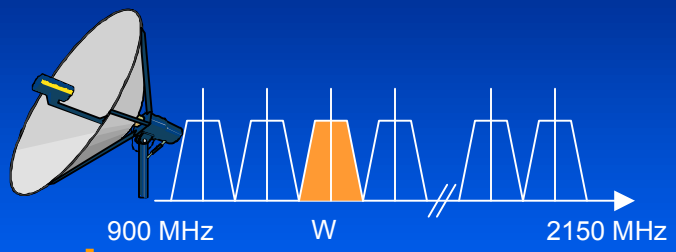
Motivation

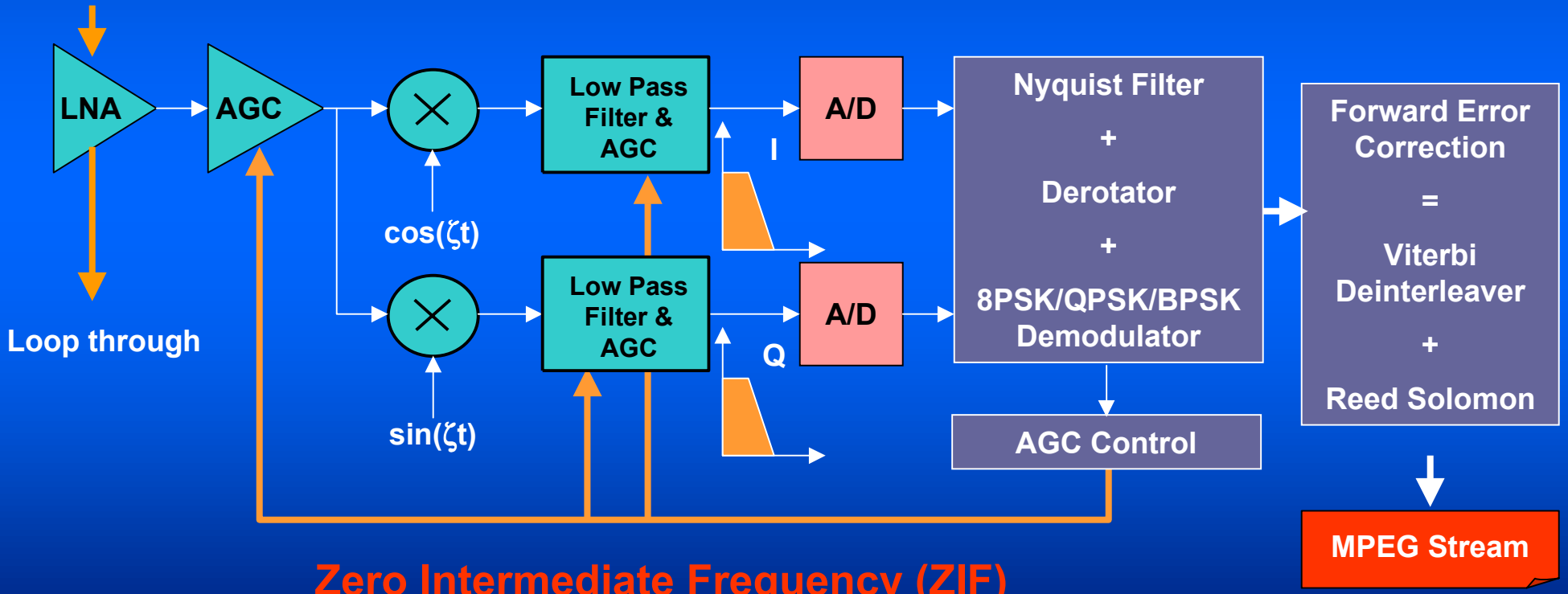
- To simulate a whole front-end RF of a single chip satellite tuner for digital TV
  - At system level:
    - To specify RF block parameters
    - To verify RFIC / Digital blocks interface
    - To study digital feedback equalization loop
  - At electrical level:
    - To evaluate performance degradation with transistor level blocks
- To define and validate a design flow based on Agilent Advanced Design System simulators

Satellite Tuner Description

- Challenging Design Objective:
  - Fully integrated tuner from RF signals to decoded digital data
  - Very low cost external components
  - Low cost CMOS process (0.18u)
- Integrated System Architecture:
  - Analog/RF design constraints traded with digital architecture
  - RF/analog blocks, ADC,digital blocks, frequency synthesizers
- Main features:
  - Input frequency bandwidth: 900 – 2150 MHz
  - Zero IF integration
  - Multi standard link (B/Q/8 PSK) : symbol rate from 1 to 30 Mbauds
  - Analog part (including ADC and PLL): 15000 devices
  - Digital part: 200K Gates, Clock frequency up to 150MHz

Block diagram

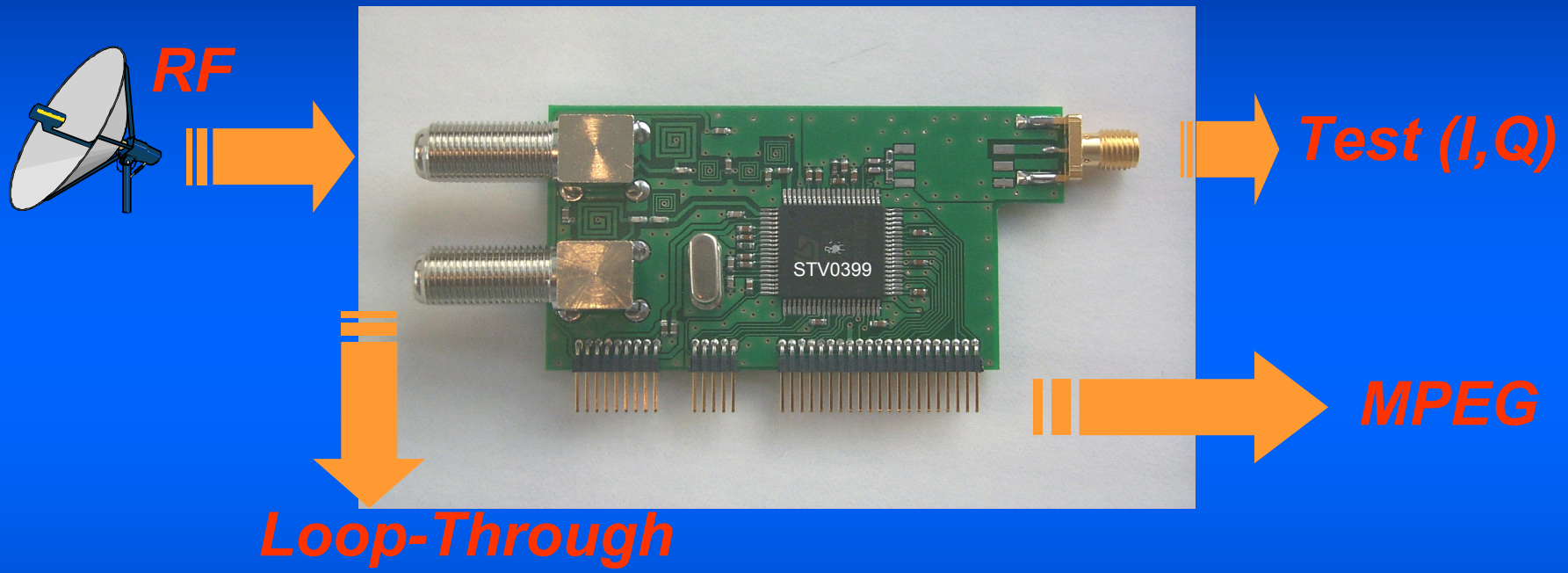




Zero Intermediate Frequency (ZIF)

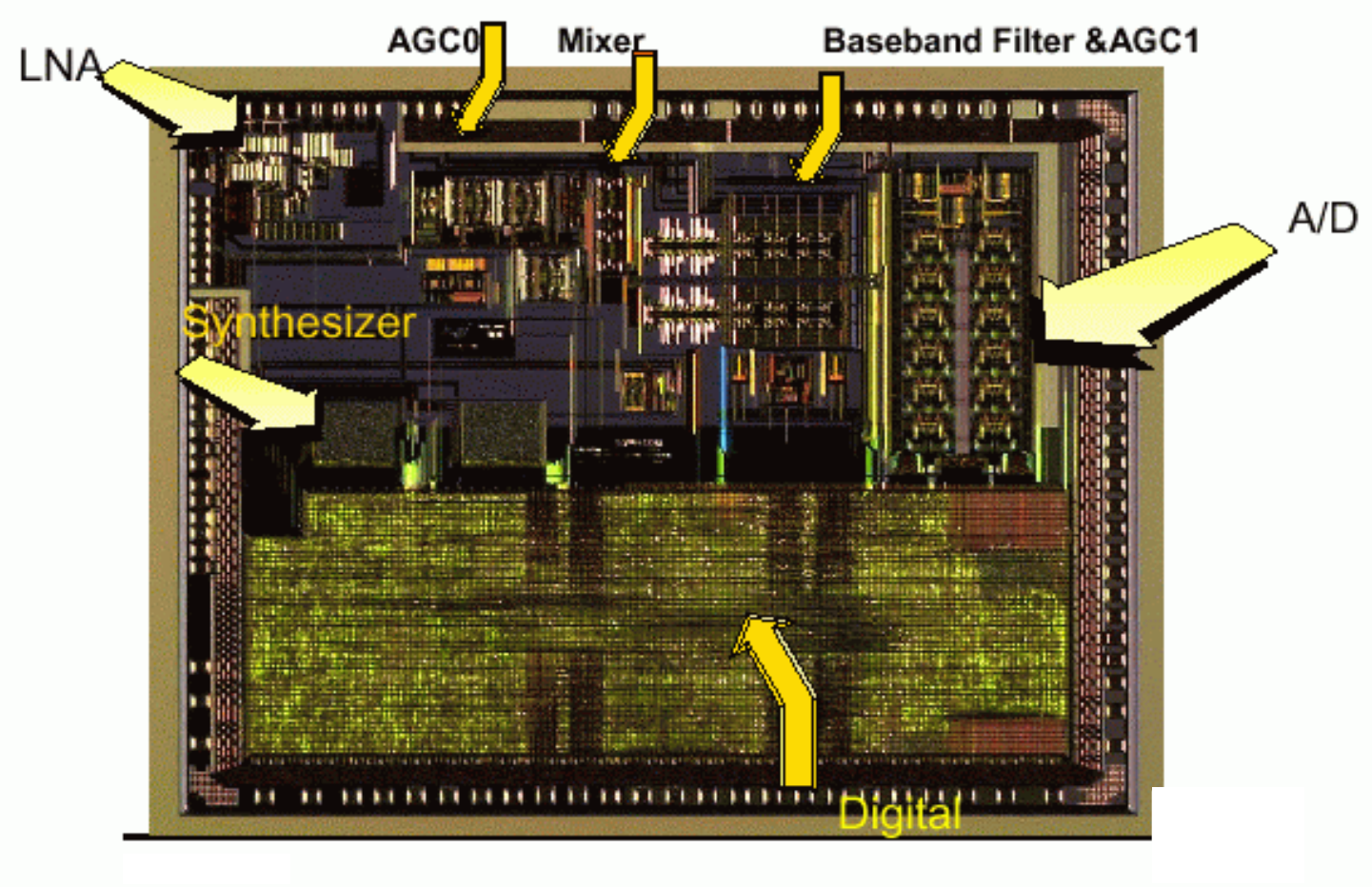
Architecture with AGC equalization

STV0399 board
RF input to MPEG data stream



- Very few external components
- Board size = 60mm x 45mm (die size = 16 mm2)
- Very low sensitivity to other RF signals
- 27 MHz crystal

STV0399 chip picture



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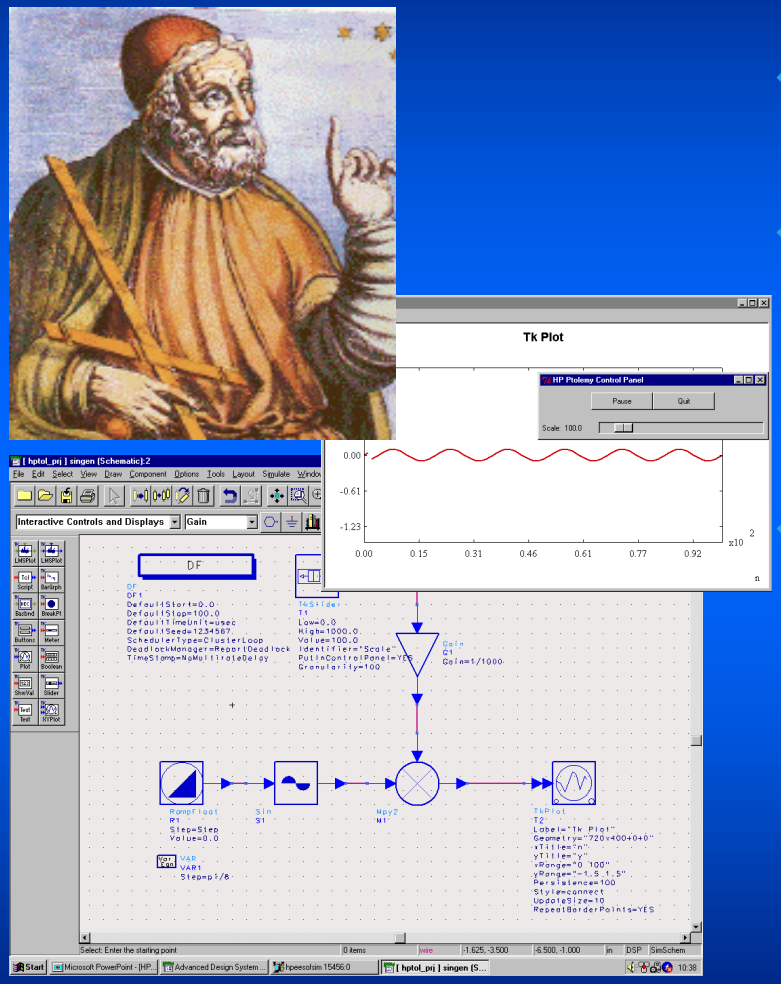
- **ADS platform**
  - Digital co-simulation
  - Circuit envelope
- Simulation results
- Conclusion

Agilent Ptolemy

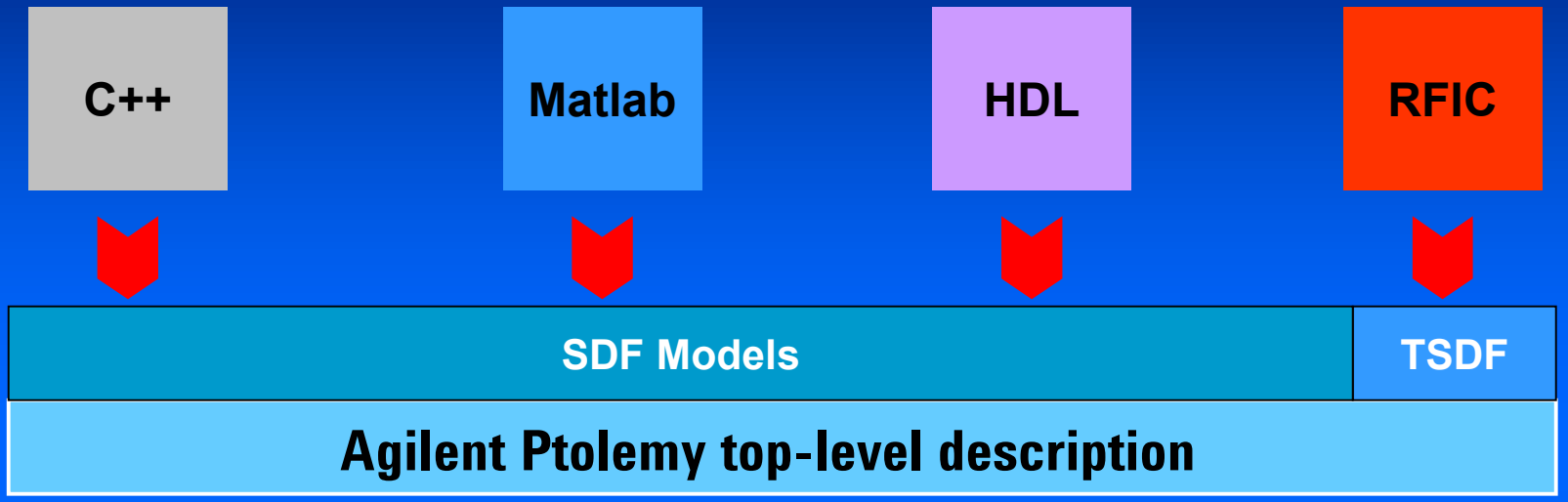


- Based on the Ptolemy code from UC Berkeley
- ADS Ptolemy uses the Synchronous Dataflow (SDF) domain for Digital Signal Processing analysis
- Agilent enhancements:
  - Timed Synchronous Dataflow (TSDF) domain for RFIC co-simulation (Envelope)
  - Large library of behavioral and time-domain models for newest communication standards
  - I/O Interfaces: Matlab, VHDL…

ADS Ptolemy Data Flow Domains

- Synchronous Data Flow domain
  - "Tokens" (data units) are consumed (inputs) and produced (outputs) by each "actor" (functional block)
  - Schedule is constructed once and repeatedly executed
  - Digital simulator is launched for each arriving input token during a pre-defined time step
- Timed Synchronous Data Flow domain
  - Timed data tokens produced from a timed actor are equally spaced in time
  - Timed data type that can represent a signal as an envelope and carrier frequency (f_c), just like Transient and Circuit Envelope

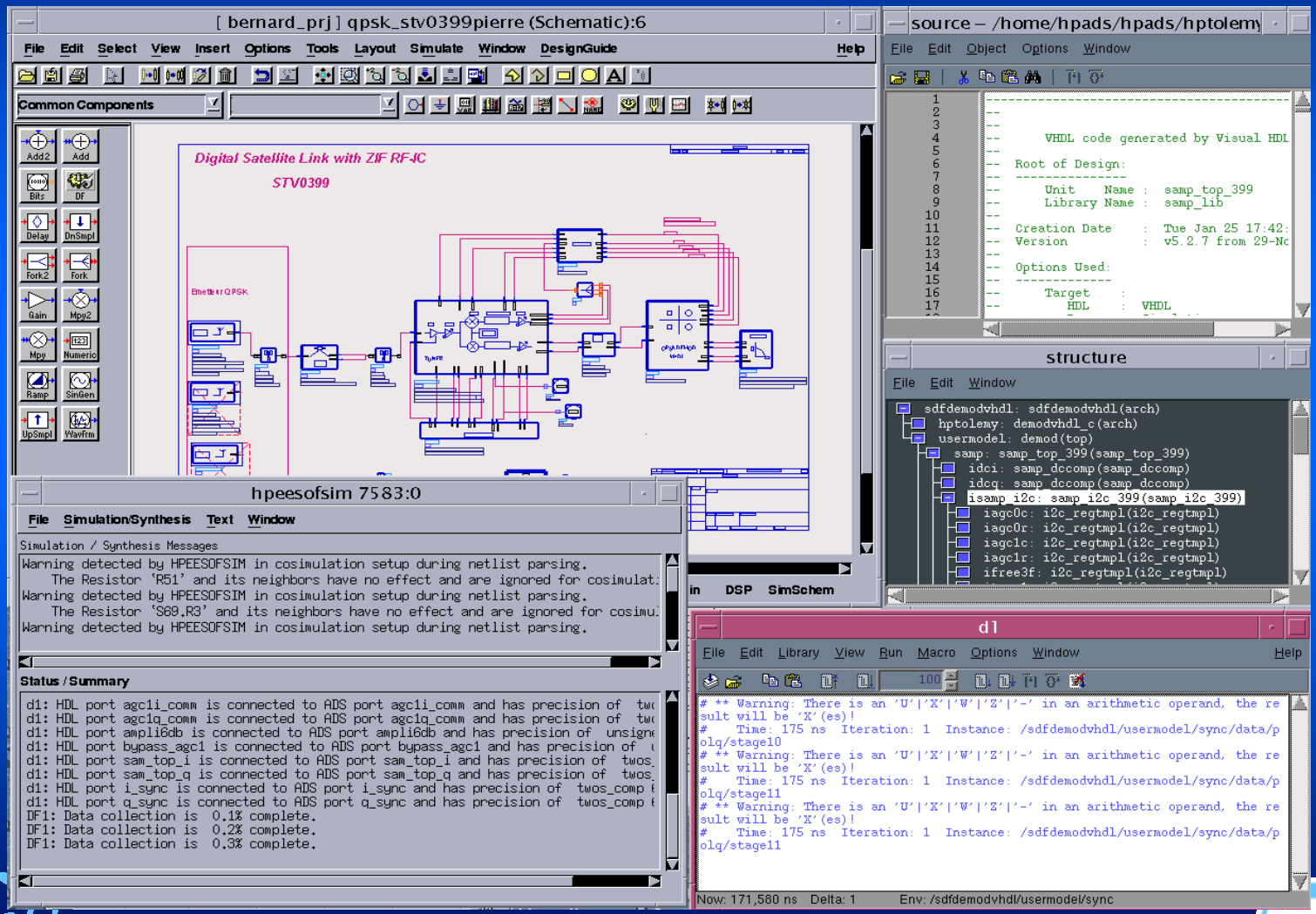
ADS Co-simulation - I/O Interfaces



ADS Ptolemy simulations can incorporate:

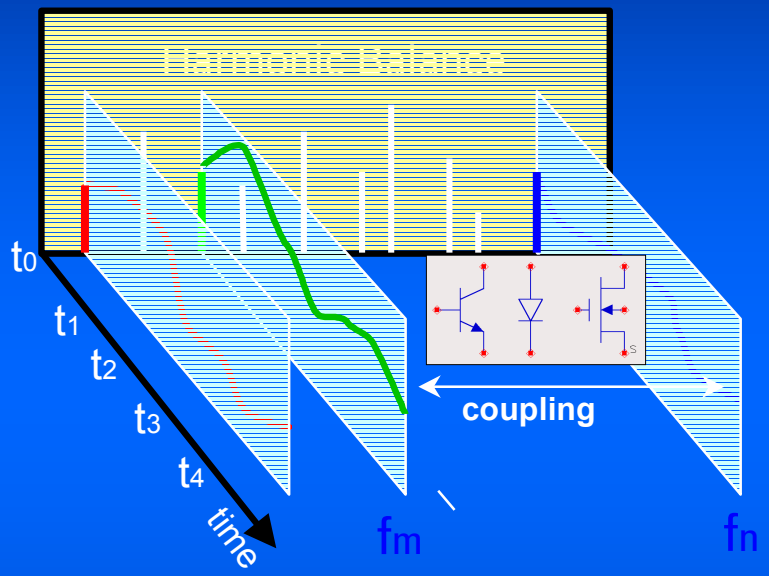
- **VHDL code** by launching Mentor Graphics **ModelSim** or Cadence **Verilog-XL** + **NCsim** digital simulators
- **Matlab** models
- **C++** code
- **RFIC** or transistor level simulators using ADS **Envelope** or **Transient** simulators

ADS and ModelSim GUI



ADS Circuit Envelope

- To co-simulate with transistor level description
- Each input signal is converted into a Fund. harmonic + a time-varying envelope
- An Harmonic Balance (HB) analysis provides the initial condition at t=0
- Modified HB equations are solved independently in the time domain, generating a complex envelope for each frequency



Fourier series with time-varying (digitally modulated) coefficients

$$v(t) = real\left|\sum_{k=0}^{N} V_k(t)e^{j\omega_k t}\right|$$

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  - System level simulations
  - Circuit level simulations
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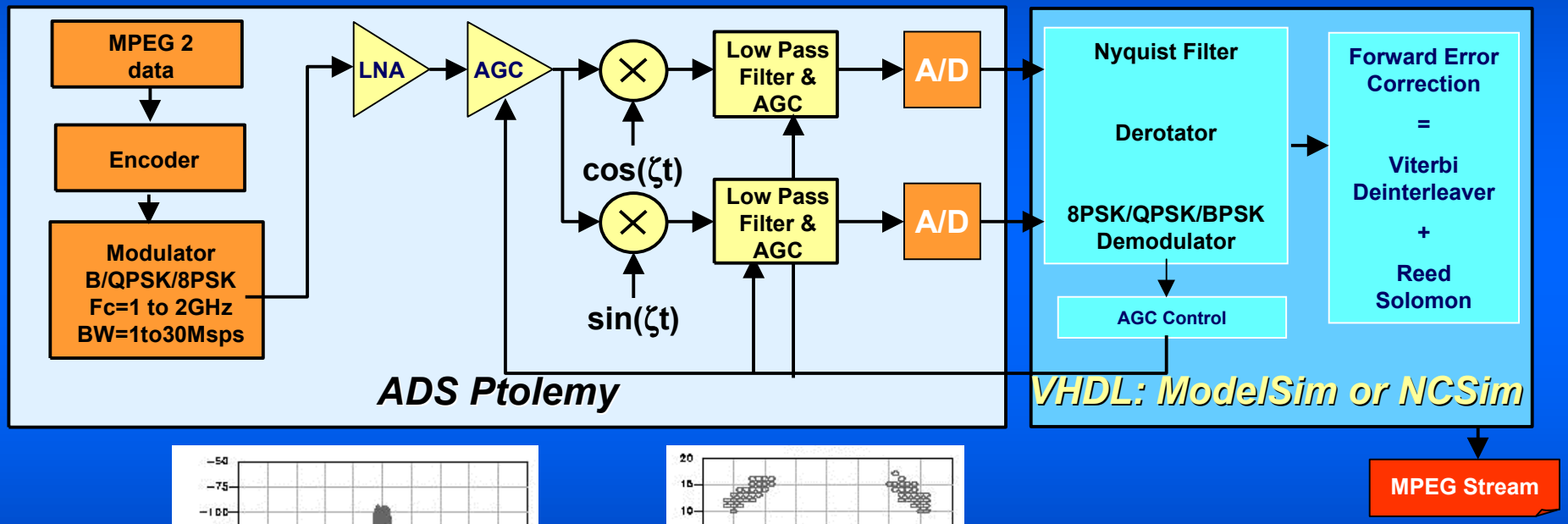
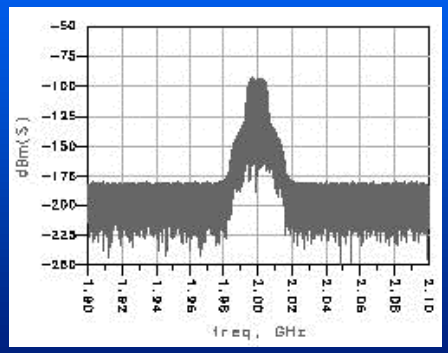
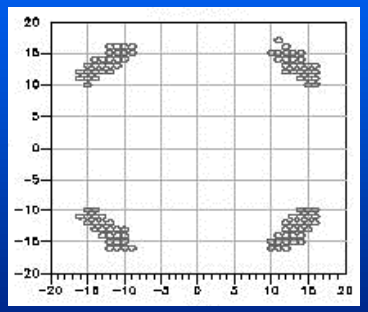
System simulation of the STV0399

Simulation of the entire signal path from input MPEG bits to output MPEG bits into a single simulation environment





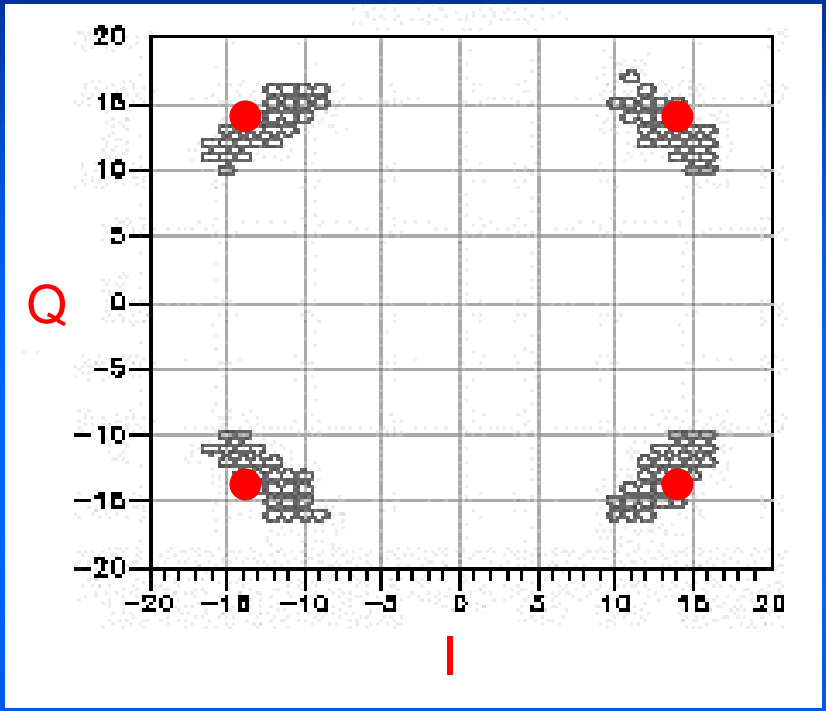
Spectrum



Constellation

Error Estimation

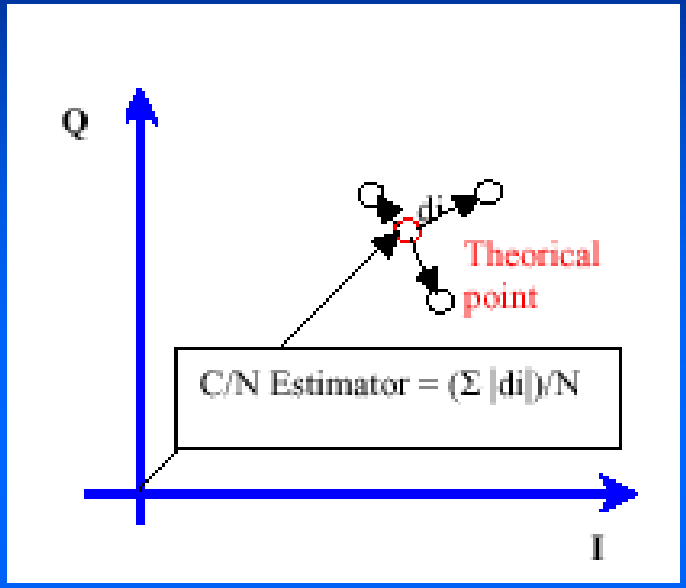
Transmission characteristics



EVM: Error Vector Magnitude

+

BER: Bit Error Rate



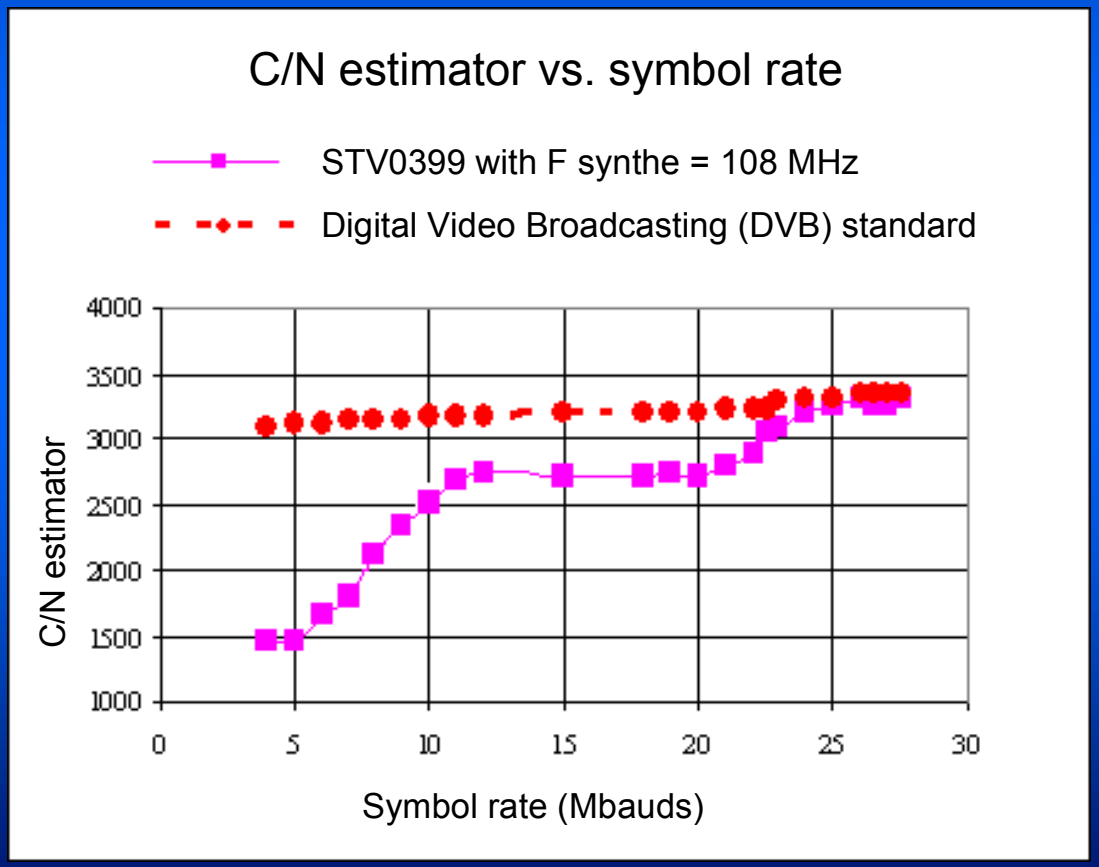
C/N Estimator

Carrier to Noise Estimator is computed internally by the digital part using a look-up table. It can be correlated to SNR:

2000 -> SNR = 23dB

Simulation vs. Measurement

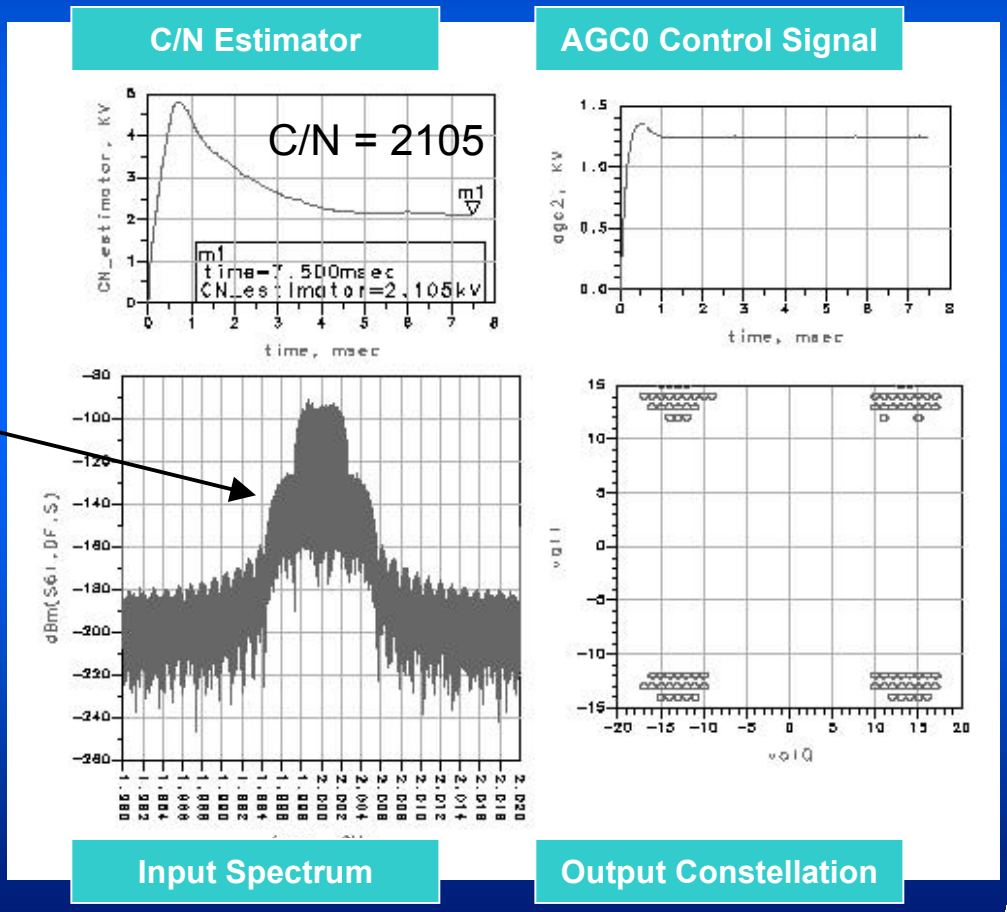
Carrier to Noise Estimator versus symbol rate compared with DVB_S standard



Parasitic noise simulation

Symbol rate = 4 Mbauds Time = 30000 symbols

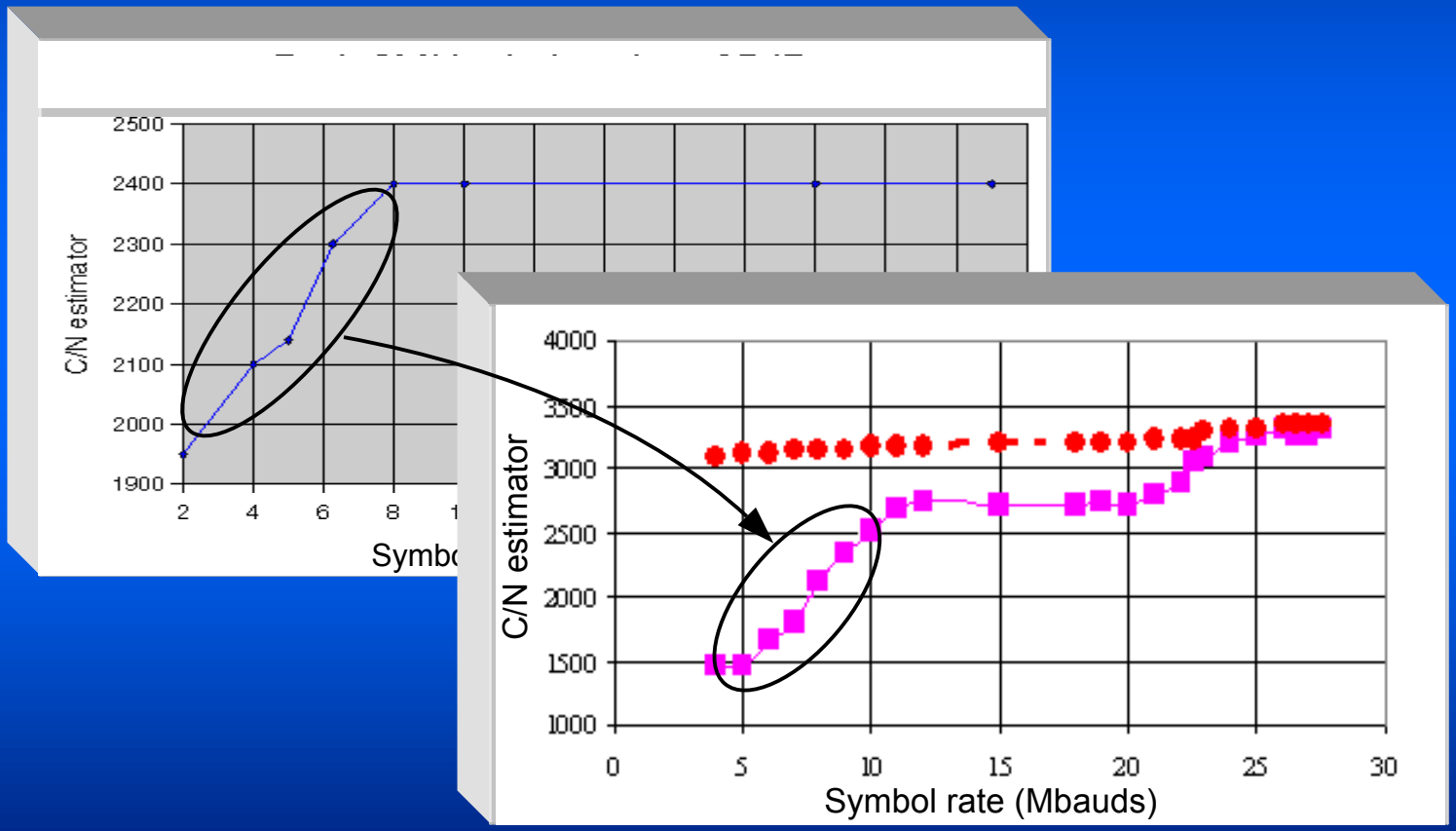
8 MHz bandwidth
noise added (-25 dBc)



Parasitic noise simulation

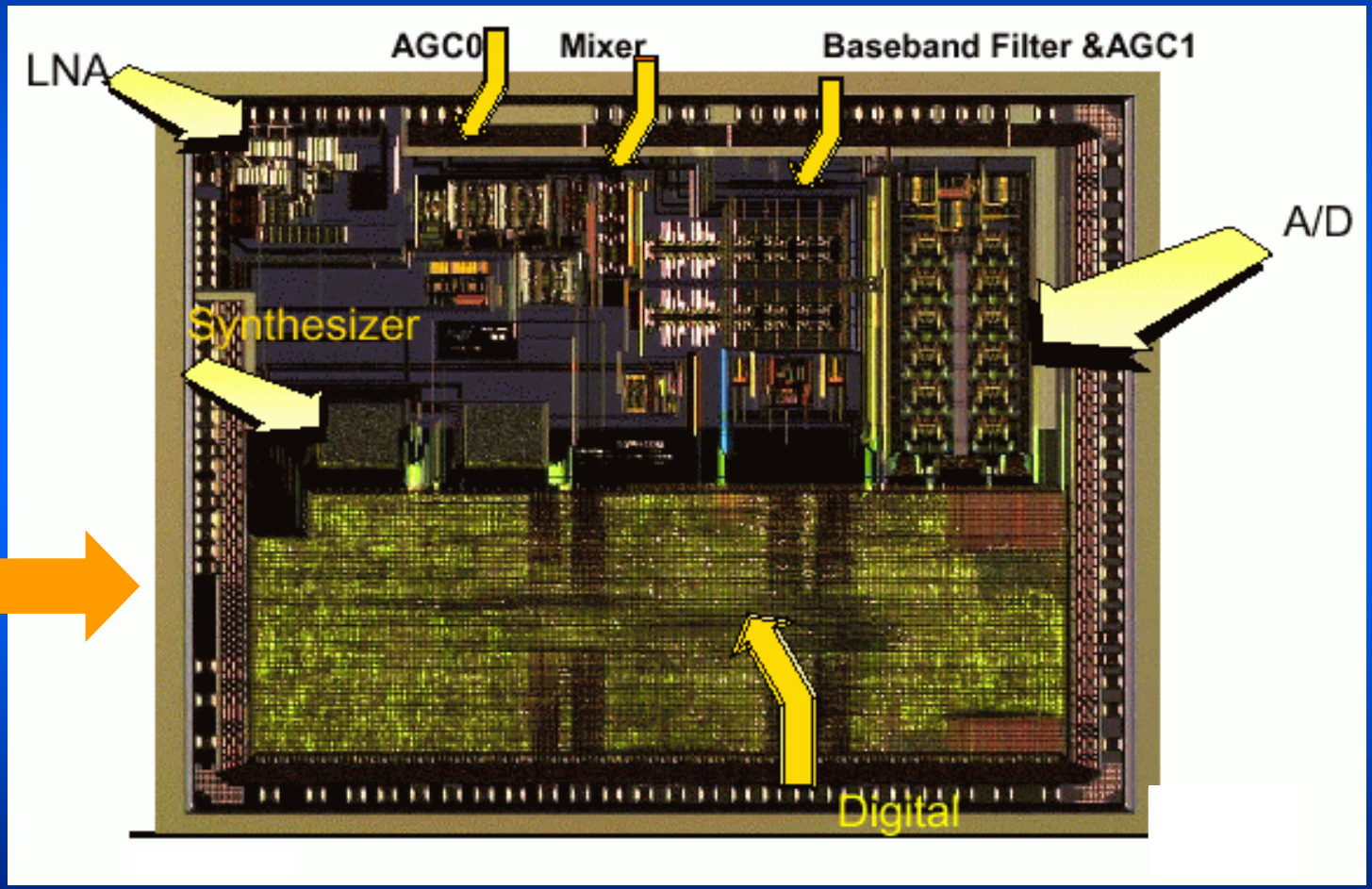
Time = 30000 symbols for each symbol rate

ADS simulations



Measurement

Clock spurious



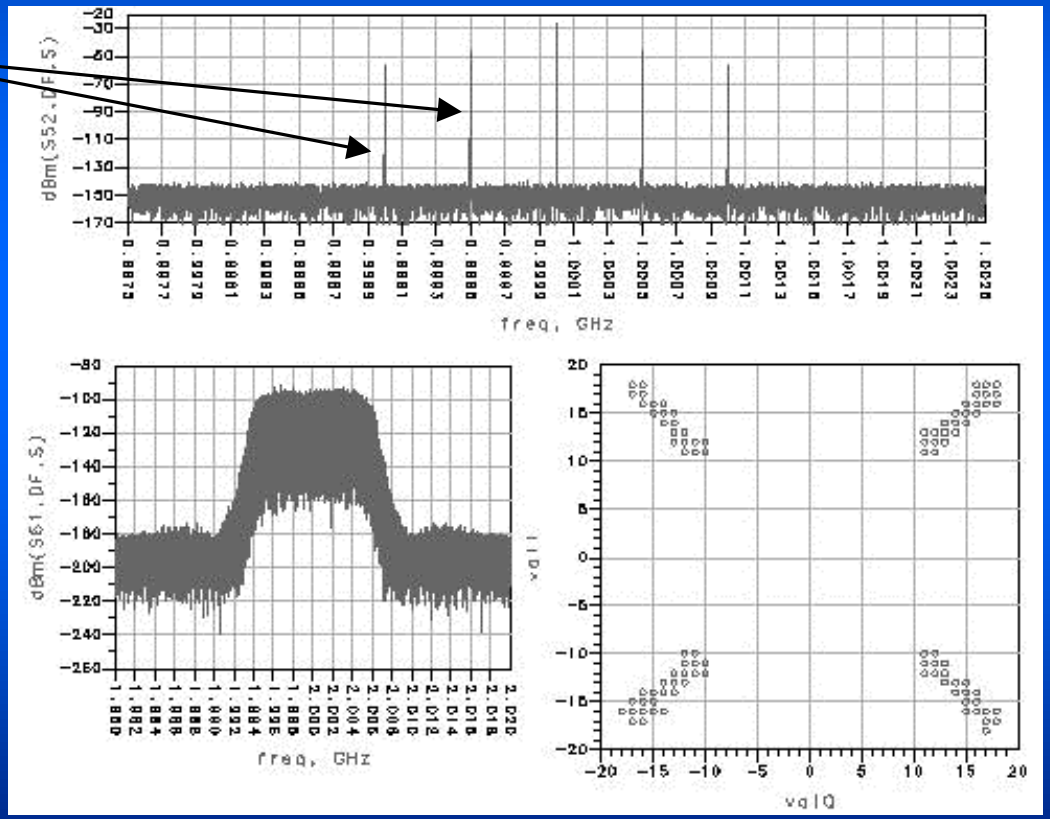
27 MHz crystal

Clock spurious

Symbol rate = 27.5 Mbauds Time = 30000 symbols

PLL spectrum

Spurious



Input spectrum

Output constellation

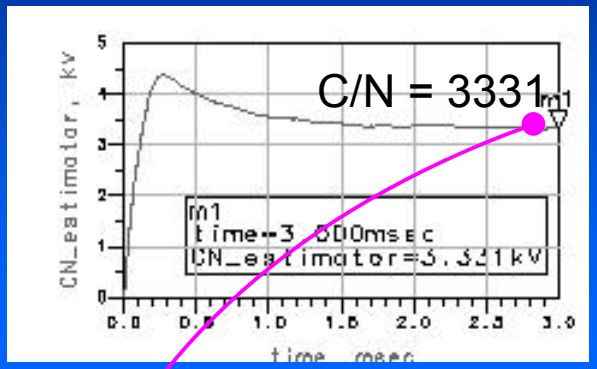
$F_{crystal}$ = 27 MHz

F_{rate} = 27.5 MHz

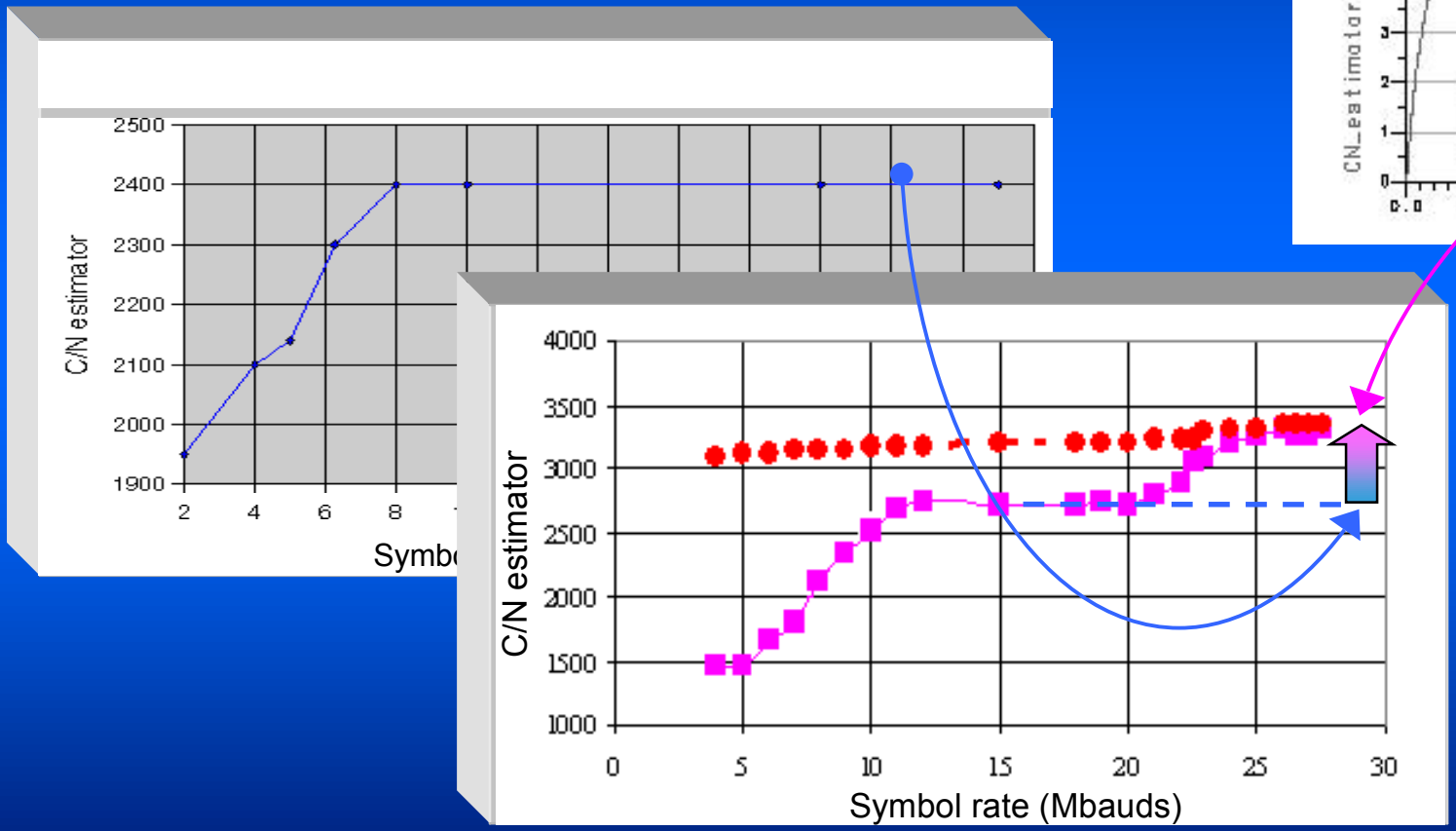
Some spurious appear at 500 kHz and degrade the performances.

Clock spurious

ADS simulations with spurious



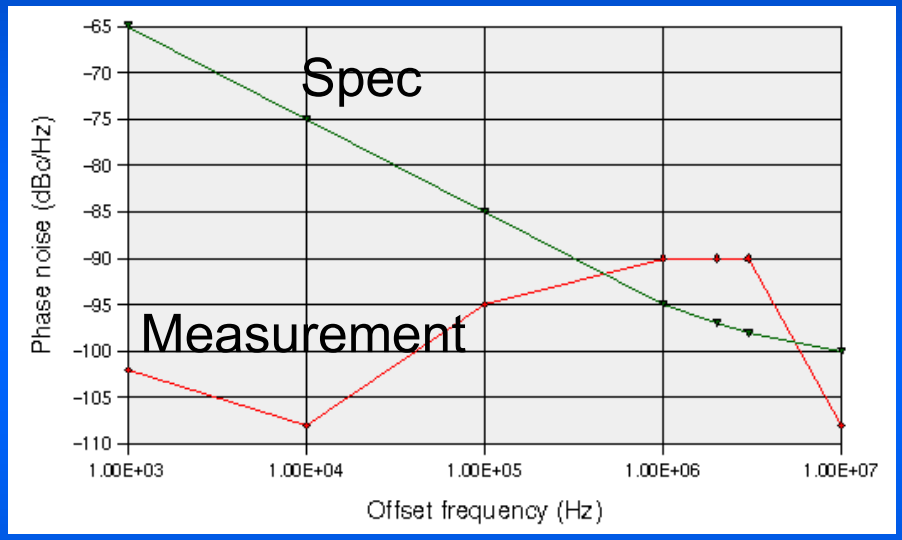
ADS simulations without spurious



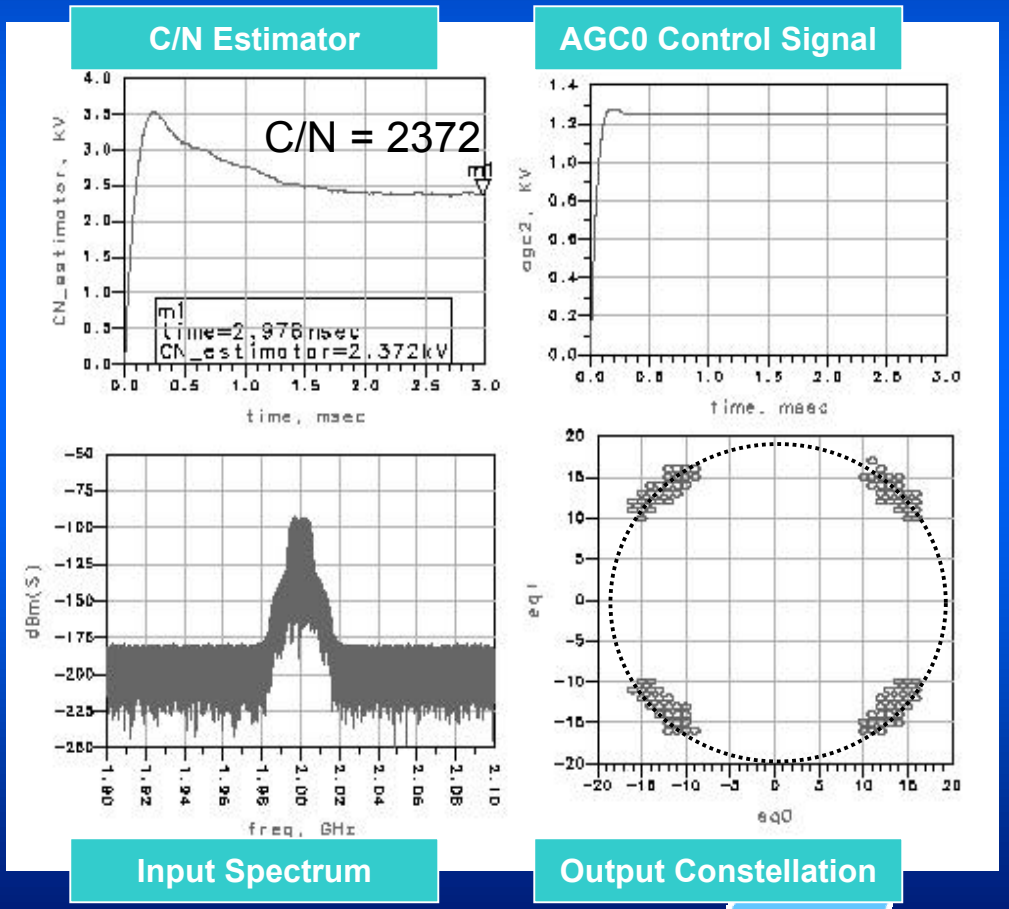
Measurement

Phase noise simulation

Symbol rate = 6.25 Mbauds Time = 30000 symbols

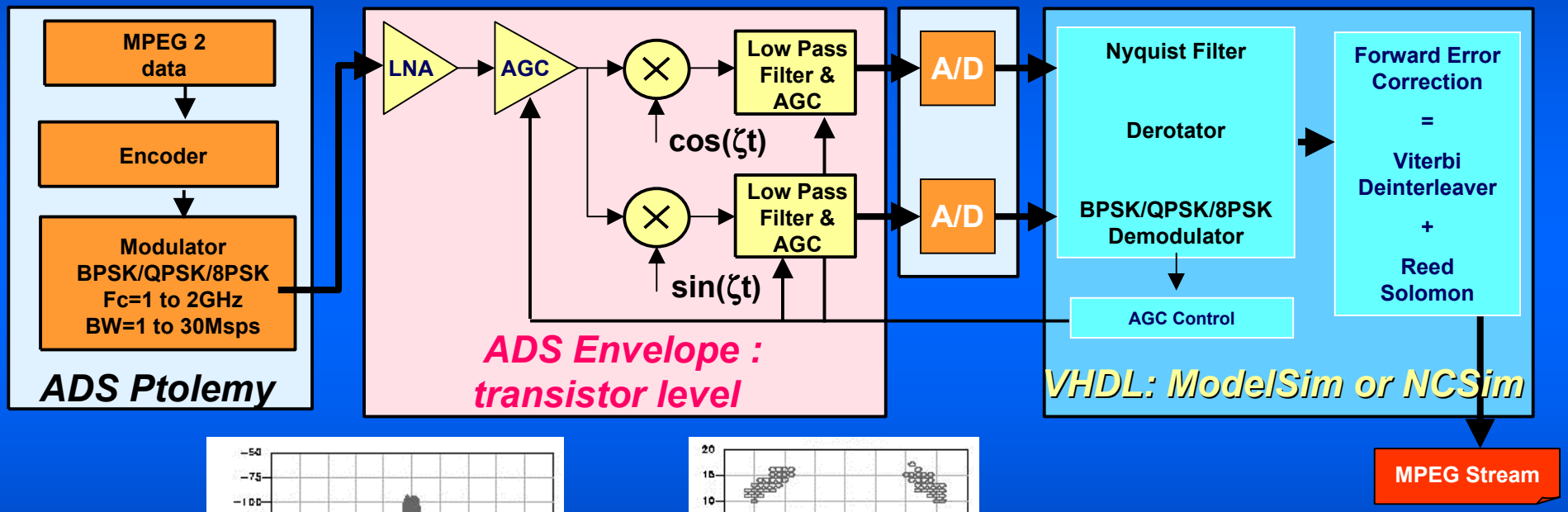


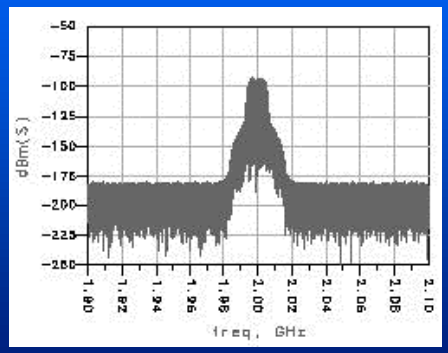
Measured phase noise was added in ADS simulations



Circuit simulation of the STV0399

Simulation of the entire signal path from input MPEG bits to output MPEG bits into a single simulation environment





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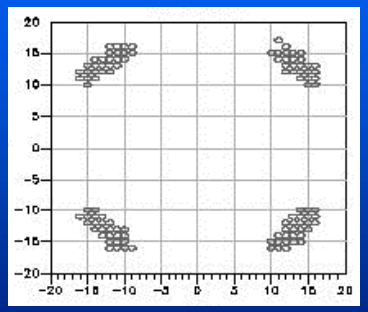
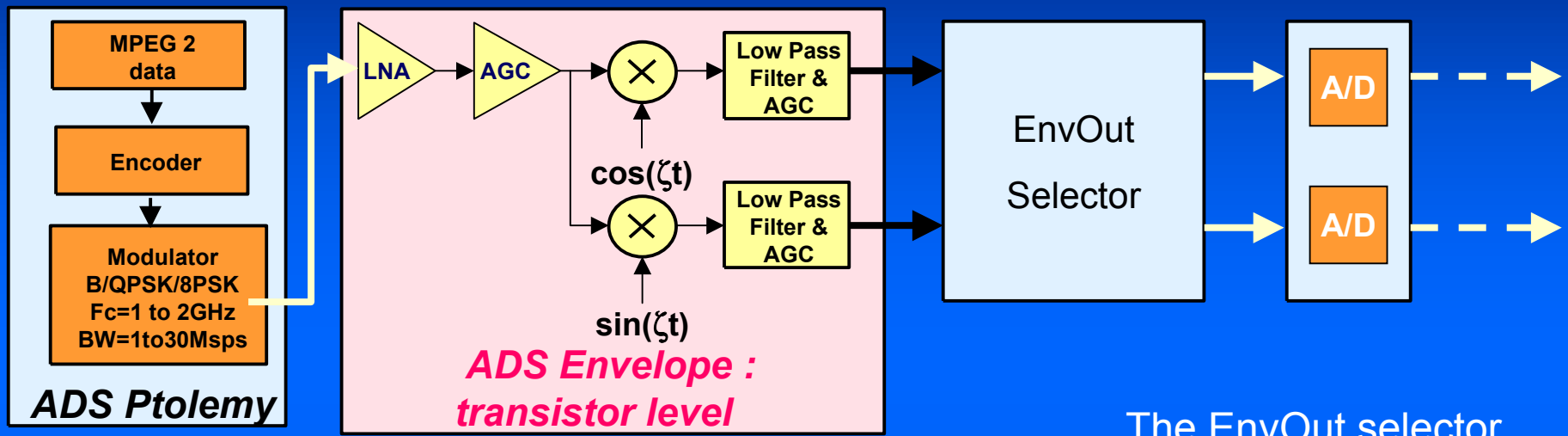


Constellation

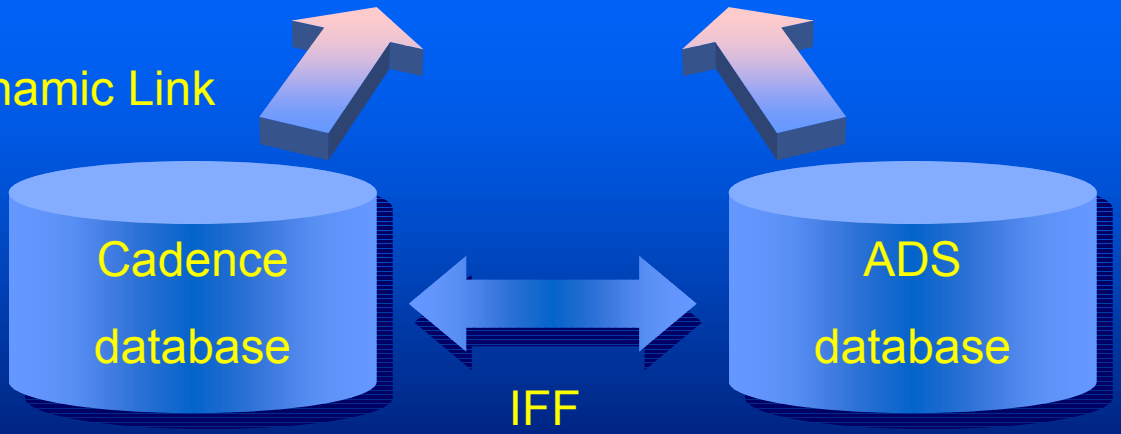
Error Estimation

Circuit simulation of the STV0399

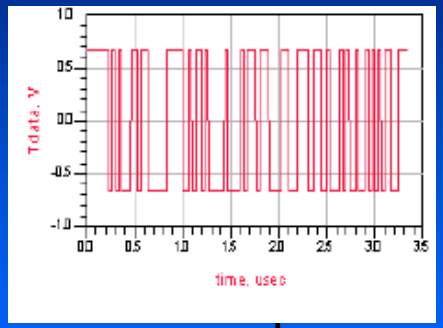


The EnvOut selector allows to choose the carrier frequency

RFIC Dynamic Link



Circuit simulation : time-domain results



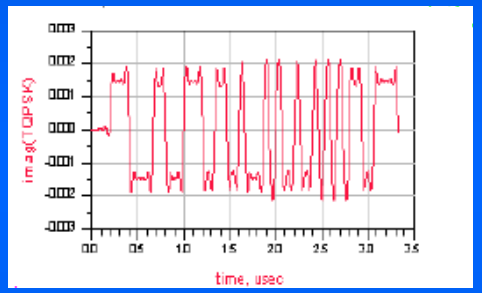
Input bit stream

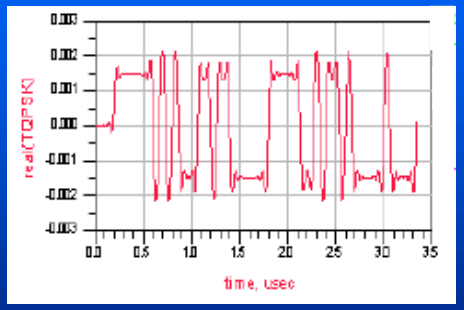
MPEG 2 data

Encoder

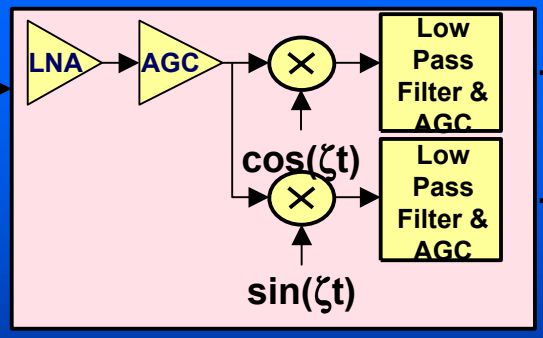
Modulator
B/QPSK/8PSK
Fc=1 to 2GHz
BW=1to30Msps

ADS Ptolemy



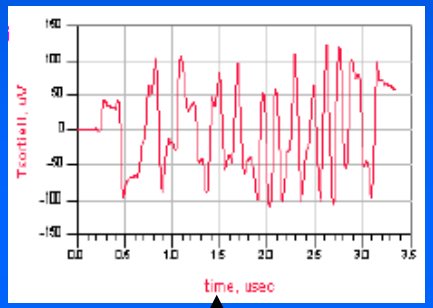


Modulated signal

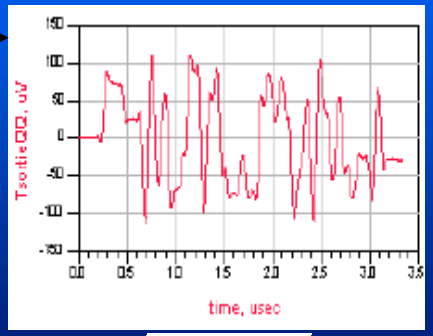


ADS Envelope : transistor level

I channel



Q channel



Circuit level simulation

Aim : To see « real life » designs impact on performances.

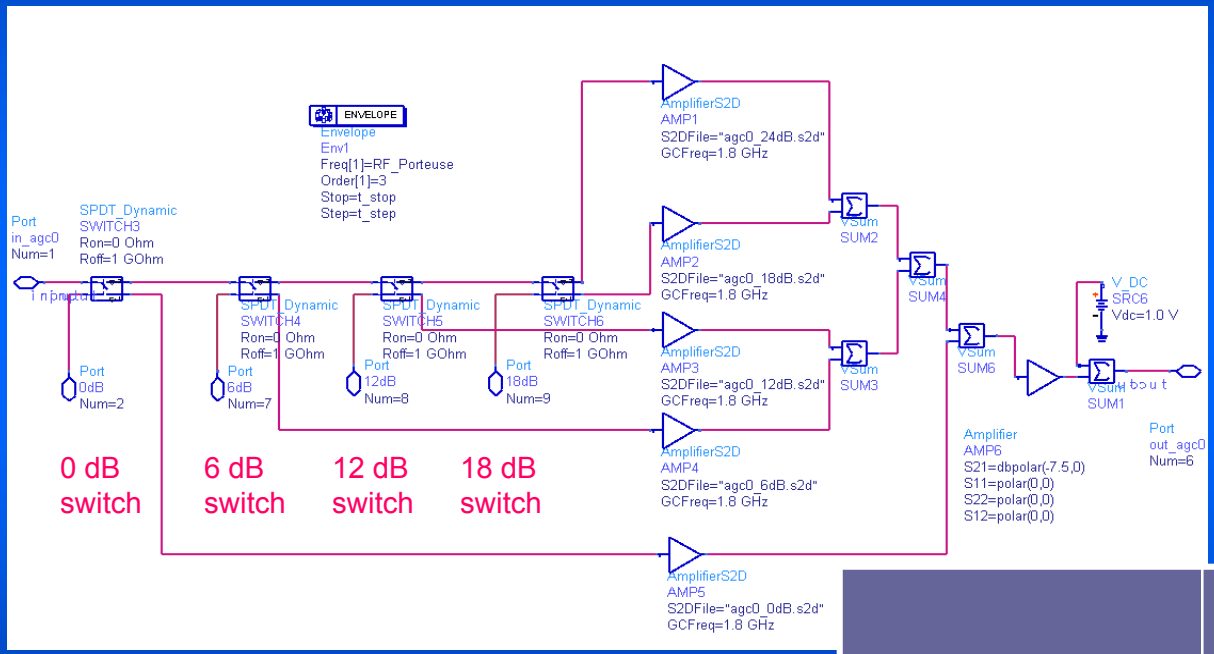
BUT real time consuming task

	System level amplifier	Transistor level amplifier
CPU Time Ratio	**1 x = 47 mn**	**29 x**

… Find a trade-off between speed and accuracy …

Behavioral models

Aim : To save time without loss of accuracy



Used accurate table-based models derived from standard simulations

	System level amplifier	« Model » level amplifier
CPU Time Ratio	**1 x**	**1.6 x**

What we learnt…

- Agilent Advanced Design System let simulate a whole front-end RF of a satellite receiver for digital TV
  - At system level using ADS Ptolemy SDF and ModelSim VHDL simulators
  - At electrical level using ADS Envelope simulator and table based behavioral models to speed-up simulation
  - Good correlation between simulation and measurements
  - Improved the design itself
  - Allowed to explain some problems found in measurement phase

What we learnt…

- However, simulation times are still very long
  - for BER estimation
  - including phase noise
  - and RFIC co-simulation
- Need Agilent tools to easily extract table-based models
- Next ST developments using ADS as reference platform: cable, terrestrial, home television wireless distribution (HiperLAN2: 6GHz WLAN)...